Claims

What is claimed and desired to be secured by Letters Patent is:

1. A memory device comprising:

a synchronous controlled global element; and

a self-timed local element interfacing with said synchronous controlled global element.

2. The memory device of Claim 1, wherein said global element includes a global predecoder.

3. The memory device of Claim 1, wherein said global element comprises at least one global decoder.

4. The memory device of Claim 1, wherein said global element comprises at least one global controller.

5. The memory device of Claim 1, wherein said global element comprises at least one global sense amplifier.

6. The memory device of Claim 1, wherein said local element comprises a plurality of memory cells forming at least one cell array.

7. The memory device of Claim 1, wherein said local element comprises at least one local decoder.

8. The memory device of Claim 1, wherein said local element comprises at least one local sense amplifier.

9. The memory device of Claim 1, wherein said local element comprises at least one cluster.

10. The memory device of Claim 1, wherein said local element comprises at least one block.

11. The memory device of Claim 1, wherein said block comprises at least one sub-block.

12. The memory device of Claim 1, wherein said local element comprises:

a plurality of memory cells forming at least one cell array;

at least one local decoder interfacing with said at least one cell array;

at least one local sense amplifier interfacing with said local decoder and said cell array and adapted to precharge and equalize at least one line coupled thereto; and

at least one local controller interfacing with and coordinating at least said local decoder and sense amplifier.

13. The memory device of Claim 12, wherein said local element further comprises at least one cluster.

14. A synchronous self-timed memory structure comprising:

a plurality of memory cells forming at least one cell array;

at least one local decoder interfacing with said at least one cell array;

at least one local sense amplifier interfacing with at least said one decoder and said cell array and adapted to precharge and equalize at least one line coupled thereto; and

at least one local controller interfacing with and coordinating said local decoder and sense amplifier.

15. The memory structure of Claim 14, further including at least one line replicating a global bit line interfacing with said local controller.

16. The memory structure of Claim 14, wherein said local sense amplifier is adapted to multiplex at least two sense amplifiers.

17. The memory structure of Claim 14, wherein said local sense amplifier is adapted to multiplex four sense amplifiers to a multiplexed line coupled to said local sense amplifier.

18. A memory device comprising:

a muxing device; and

at least one cluster device coupled to said muxing device.

19. The memory device of Claim 18, wherein said cluster device is adapted to sink all local sense amps contained in said cluster device.

20. The memory device of Claim 18, further comprising a plurality of local clusters having a common local wordline coupling all said clusters in block.

21. The memory device of Claim 18, wherein said cluster includes at least one sense amplifier adapted to be activated by a global cluster line.

22. A hierarchical memory structure that comprises a logical portion of a larger memory device, the hierarchical memory structure comprising:

a plurality of memory cells forming at least one cell array;

at least one local decoder interfacing with said at least one cell array;

at least one local sense amplifier interfacing with said at least one decoder and said at least one cell array and adapted to precharge and equalize at least one line coupled thereto; and

at least one local controller interfacing with and coordinating said at least one local decoder and said at least one sense amplifier.

23. A sense amplifier device having at least one sense amplifier and adapted to be used in a memory device comprising:

a precharging and equalizing device adapted to precharge and equalize unused lines at a predetermined value; and

at least one transistor adapted to isolate the sense amplifier.

24. The sense amplifier device of Claim 13, further including at least one PMOS transistor adapted to isolate the sense amplifier from a global bit line.

25. A method of performing a read operation using a memory device containing at least one logical memory subsystem, the method comprising:

selecting at least one cell array;

selecting at least one sub-block in the logical memory subsystem;

isolating at least one local sense amplifier;

activating a local wordline;

discharging at least one bitline in at least one bitline pair;

developing a differential voltage across said bitline pair;

stopping said discharge; and

equalizing and precharging said bitline pair.

26. The method of Claim 25, further comprising activating at least one mux line to select said cell array.